REMARKS

The claims are claims 1 to 12.

Claims 8 to 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Pawate et al U.S. Patent No. 5,638,530.

Claim 8 recites subject matter not anticipated by Pawate et al. Claim 8 recites "selecting a first portion of the memory circuit responsive to a size parameter stored in a register, such that a second portion of the memory circuit is not selected; and limiting access to the first portion of memory circuit to only a first requestor of the plurality of requestors when the digital system is in a second mode of operation." Pawate et al has no such teaching or suggestion to select a first portion of memory in accordance with a size parameter and to limit access to the selected portion. Pawate et al clearly teaches at column 13, lines 29 to 35 that arbitration is required unless the DSP is turned off "Since both the DSP and the host computer access the shared memory on the smart card, bus arbitration is necessary. If the host computer attempts to access the shared memory, the operation of the DSP is halted." Pawate et al teaches at column 13, lines 49 to 52 "If the CLKON bit is set to zero, the DSP (120) is placed in a hold state, forcing the buses of the DSP (170) to be tri-stated and allowing the host computer to have free access to the common memory (150).

Pawate et al does teach use of a control register that provides limited access: Pawate et al states at column 13,. lines 35 to 39 "However, since the communication control and control registers are not resident in the shared memory, but in fact are resident in the interface and control circuit (180), access, write or read to these registers by the host computer does not halt the operation of the DSP." These control registers are not shared and

are not relevant to the present claims. Therefore, Claim 8 is allowable over Pawate et al.

Claim 9 recites subject matter not anticipated by Pawate et al. Claim 9 recites "sharing access to the second portion of the memory circuit between the plurality of requestor circuits when the digital system is in the second mode of operation." Pawate et al teaches at column 6, lines 47 to 49 "While the smart card is in the standard mode, the DSP is inactive." Pawate et al also reaches at column 13, line 30 while in smart mode, "bus arbitration is necessary." Thus, Pawate et al does not suggest a mode where a first portion of the memory is limited to one requester while the second portion is shared. Claim 9 is therefore allowable over Pawate et al.

Claim 10 recites subject matter not anticipated by Pawate et al. Claim 10 recites "placing the second portion of the memory circuit in a low power mode when the digital system is in the second mode of operation." Pawate et al does not teach placing the second portion of the memory circuit in a low power mode when the digital system is in the second mode of operation. Instead, Pawate et al teaches at column 14, lines 6 to 8 "turn off the clock of the DSP" to minimize power. This power down disclosed in Pawate et al is of a different structure than claimed. Pawate et al does not suggest powering down a portion of the memory since the host is given access to the memory when the DSP is powered down. Claim 10 is therefore allowable over Pawate et al.

Claims 1 to 7 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Boutaud et al U.S. Patent No. 5,838,934 and Pawate et al U.S. Patent No. 5,638,530.

Claim 1 recites subject matter not made obvious by the combination of Boutaud et al and Pawate et al. Claim 1 recites "select a first portion of the memory circuit in response to the

size parameter when the access mode circuitry indicates the second access mode, wherein only the first portion of the memory circuit is operable for exclusive access by the first requestor when the access mode circuitry indicates the second access mode." As discussed above, Pawate et al has no teaching or suggestion to select a first portion of memory in accordance with a size parameter and to limit access to the selected portion, as claimed in Claim 1. Likewise, Boutaud et al has no such teaching. Boutaud et al does have a shared access mode (SAM) and a host only mode (HOM). Boutaud et al teaches at column 8, line 59 to column 9, line 7 that the entire memory circuit 200 is treated as a single portion and is either entirely in host only mode or in shared access mode. Neither Boutaud et al nor Pawate et al suggest "a size register for holding a size parameter coupled to the selection circuit, the selection circuit being operable to select a first portion of the memory circuit in response to the size parameter when the access mode circuitry indicates the second access mode, wherein only the first portion of the memory circuit is operable for exclusive access by the first requestor when the access mode circuitry indicates the second access mode" as recited in Claim 1. Claim 1 is therefore allowable over the combination of Boutaud et al and Pawate et al.

Claim 2 recites subject matter not made obvious by the combination of Boutaud et al and Pawate et al. Claim 2 recites "a second portion of the memory circuit not selected in response to the size parameter is operable to be in a low power mode when the access mode circuitry indicates the second access mode." Pawate et al does not teach placing the second portion of the memory circuit in a low power mode when the access mode circuitry indicates the second mode of operation. Pawate et al instead teaches at column 14, lines 6 to 8 to "turn off the clock of the DSP" to minimize power. This is a different structure than that recited in claim 2.

Pawate et al does not suggest powering down a portion of the memory since the host is given access to the entire memory when the DSP is powered down. Claim 2 is therefore allowable over the combination of Boutaud et al and Pawate et al.

Claim 3 recites subject matter not made obvious by the combination of Boutaud et al and Pawate et al. Claim 3 recites "a second portion of the memory circuit not selected in response to the size parameter can be accessed by the second requestor when the access mode circuitry indicates the second access mode." Pawate et al teaches at column 6, lines 47 to 49 "While the smart card is in the standard mode, the DSP is inactive." Accordingly, in the second mode the inactive DSP cannot access the second portion of the memory as recited in claim 3. Accordingly, claim 3 is allowable over the combination of Boutaud et al and Pawate et al.

Claim 4 recites subject matter not made obvious by the combination of Boutaud et al and Pawate et al. Claim 4 recites "the size parameter is ignored when the access mode circuitry indicates the first access mode such that the entire memory circuit is operable to be selected for sequential access by the first requestor and the second requestor." Neither Pawate et al nor Boutaud et al suggest a size parameter for selecting a portion of the memory. Thus neither can suggest ignoring the size parameter as recited in claim 4. Accordingly, claim 4 is allowable over the combination of Boutaud et al and Pawate et al.

The Applicants respectfully request entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment serves only to clarify subject matter previously recited. Thus no new search or reconsideration is required.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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